CERTIFICATE OF EXPRESS MAILING

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Gedney et al.	
Serial No: To be assigned	Art Unit: Unknown
Filed: Herewith	Examiner: Unknown
For: **IC CHIP ATTACHMENT**	
Reissue of U.S. Patent No. 5,483,421	Attorney's Docket No: EN9-91-022R (21325/00276)
Issued: January 9, 1996	

DECLARATION OF RONALD W. GEDNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Ronald W. Gedney ("Declarant") states and declares that:

1. He is a U.S. citizen, residing at 19970 Alexandra's Grove Road, Ashburn, VA 20147, which is also his post office address.

2 He believes that he is an original, first and joint inventor of the subject matter that is disclosed and claimed in U.S. Letters Patent No. 5,483,421 for IC Chip Attachment, issued on January 9, 1996 (the "`421 patent"), and in the enclosed specification, and for which invention he solicits a reissue patent.

3. He believes that Tamar A. Powers (formerly Tamar A. Sholtes) is a U.S. citizen residing at 509 African Road, Vestal, New York 13850, which is also her post office address, and

believes her to be the other original, first and joint inventor of the aforesaid invention.

4. He has reviewed and understands the contents of the specification of the reissue application submitted herewith, including the claims.

5. He acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR 1.56.

6. He believes that the original `421 patent is wholly or partly inoperative by reason of the patentee claiming less than they had the right to claim in the patent because all the claims were limited to packages and methods for mounting integrated circuit chips to an organic glass-filled epoxy dielectric having a coefficient of thermal expansion of at least 17 x 10^{-6} ppm/°C. All errors being corrected in the enclosed reissue application arose without any deceptive intent on the part of the applicants.

7. The invention disclosed and claimed in the `421 patent was conceived when he and the aforesaid Tamar A. Sholtes, his co-inventor, were members of a team at IBM's Endicott facility working on direct chip attachment. We realized that recent developments in encapsulation technology had made it possible to mount integrated circuit chips on chip carriers with higher coefficients of thermal expansion ("CTEs") than previously thought possible. These developments allowed us to consider building chip carriers out of organic dielectric materials such as glass-filled epoxies (commonly referred to as FR-4 materials) frequently used for printed circuit board or cardstock, or polyimides frequently used in tape automated bonding. We prepared an Invention Disclosure describing this invention (a copy of which is enclosed, with certain dates and other non-material information redacted) and submitted it to the IBM IP Law Department for consideration. The Invention Disclosure focuses on the advantages of making chip carriers of FR-4 or polyimide materials, and ways of doing this with standard processing technology. In describing stresses created by the use of materials with different coefficients of thermal expansion, the

Invention Disclosure noted that ceramic chip carriers typically have CTEs of 6-7 x 10^{-6} ppm/°C, and that the second level carrier (e.g. circuit board) to which the ceramic chip carrier is attached is typically FR-4 with a CTE of 17-20 x 10^{-6} ppm/°C. At that time Declarant was well aware that there were glass filled epoxy circuit board materials with lower CTEs and had in his possession reference materials documenting such lower figures, including an Electronic Materials Handbook published by ASM International. Declarant was a contributor to the ASM Handbook, co-authoring the article of "Hybrids and Higher Level Integration" on pages 390-96 of Section 3. Table 6 on page 536 of the Handbook, Table 1 on page 612 and Table 4 on page 616 (copies of which are enclosed) describe glass filled epoxies (FR-4) with CTEs of 11-16 x 10^{-6} ppm/°C. The figure of 17-20 x 10^{-6} ppm/°C was used for the invention disclosure because it was representative of materials typically used by IBM at that time.

8. The Intellectual Property Law Department at Endicott employed William N. Hogg of Calfee, Halter & Griswold LLP to prepare an application based on this invention. Declarant worked with Mr. Hogg, who was IBM's patent counsel at Burlington, Vermont while Declarant held the position of Manager of Packaging Development at that facility. Mounting integrated circuit chips on substrates, usually ceramic, which were then mounted on printed circuit boards was a significant part of the technical program at Burlington, and Declarant knew that Mr. Hogg generally understood this technology.

9. He reviewed a draft of the application, provided by Mr. Hogg, discussed it with Ms. Sholtes, and made comments on the draft to Mr. Hogg. They did not, however, discuss any specific levels for coefficients of thermal expansion for the organic chip carriers disclosed and claimed in the application. Mr. Hogg used the 17-20 x 10^{-6} ppm/°C figure from the Invention Disclosure in the detailed description (page 17, line 13) of U.S. Patent Application Serial No. 07/848,467 (the "`467 application") which matured into the `421 patent (this figure appears at column 7,

line 18 of this patent), but the figure was not used in any of the original claims. The broadest claims of the `467 application as filed (claims 1 and 7) were directed to packages and methods for mounting integrated circuit chips on circuit boards with chip carriers formed of an organic dielectric material and a circuit board having a coefficient of thermal expansion similar to the chip carrier. The application defines a similar coefficient of thermal expansion as meaning that differences in the coefficient of thermal expansion between the carrier and the circuit board should not vary by more than about 20% (page 15, lines 5-8 of the `467 application, column 7, lines 11-13 of the `421 patent). Original dependent claims 6 and 12 specified packages and methods wherein the coefficients of thermal expansion of the material of the chip carrier and the material of the circuit board do not differ by more than about 20%. However, none of the initial claims recited any specific coefficient of thermal expansion.

10. Sometime after the `421 Patent was issued, he was contacted by Mr. Hogg and James A. Rich, another patent attorney with Calfee, Halter & Griswold, LLP. Mr. Hogg and Mr. Rich explained that Lawrence R. Fraley, a Senior Attorney with IBM's IP Law Department at Endicott, had asked Mr. Hogg to determine if the `421 patent could be reissued to obtain broader independent claims that were not limited to coefficients of expansion of at least 17 x 10^{-6} ppm/°C. Mr. Hogg and Mr. Rich asked Declarant about his knowledge of coefficients of thermal expansion for circuit board materials at the time the Invention Disclosure for the `467 application was prepared. He explained that the figure of 17-20 x 10^{-6} ppm/°C was selected because it was representative of commercial IBM materials, but that he was well aware that glass-filled epoxy circuit board stock with lower CTEs had been produced, and provided Mr. Rich with the excerpts from the ASM International Handbook described in paragraph 7 above. Mr. Rich subsequently advised him that he and Mr. Hogg had concluded that the `421 Patent was wholly or partly inoperative by reason that the patentees had claimed less than we had the right to claim.

The claims were defective because all the claims were limited to packages and methods for mounting integrated circuit chips to an organic glass-filled epoxy dielectric having a coefficient of thermal expansion of at least 17 times 10^{-6} ppm/°C.

11. He hereby declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Ronald W. Gedney

Ronald W. Gedney

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	Attorney's Docket No: EN9-91-022R (21325/00276)
Reissue of U.S. Patent No. 5,483,421	
Issued: January 9, 1996	

DECLARATION OF TAMAR A. POWERS

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Tamar A. Powers ("Declarant") states and declares that:

1. She is a U.S. citizen, residing at 509 African Road, Vestal, New York 13850, which is also her post office address.

2. She believes that she is an original, first and joint inventor of the subject matter that is disclosed and claimed in U.S. Letters Patent No. 5,483,421 for IC Chip Attachment, issued on January 9, 1996 (the "`421 patent"), and in the enclosed specification, and for which invention she solicits a reissue patent.

3. She believes that Ronald W. Gedney is a U.S. citizen residing at 19970 Alexandra's Grove Road, Ashburn, VA 20147, which is also his post office address, and believes him to be the other original, first and joint inventor of the aforesaid invention.

4. She has reviewed and understands the contents of the specification of the reissue application submitted herewith, including the claims.

5. She acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR 1.56.

6. She believes that the original `421 patent is wholly or partly inoperative by reason of the patentee claiming less than they had the right to claim in the patent because all the claims were limited to packages and methods for mounting integrated circuit chips to an organic glass-filled epoxy dielectric having a coefficient of thermal expansion of at least 17 x 10^{-6} ppm/°C. All errors being corrected in the enclosed reissue application arose without any deceptive intent on the part of the applicants.

7. Sometime after the `421 patent was issued, she was contacted by James A. Rich, a patent attorney with Calfee, Halter & Griswold LLP. Mr. Rich explained that Lawrence R. Fraley, a Senior Attorney with IBM's IP Law Department at Endicott, had asked Mr. William N. Hogg, another patent attorney with Calfee, Halter & Griswold, LLP and attorney of record in U.S. Patent Application Serial No. 07/848,467 (the "`467 application") which matured into the `421 patent, to determine if the `421 patent could be reissued to obtain broader independent claims that were not limited to coefficients of expansion of at least 17-20 x $10^{-6}$ ppm/°C. Mr. Rich also advised her that he and Mr. Hogg had concluded that the `421 patent was wholly or partly inoperative by reason that the patentees had claimed less than we had the right to claim. The claims were defective because all the claims were limited to packages and methods for mounting integrated circuit chips to an organic glass-filled epoxy dielectric having a coefficient of thermal expansion of at least 17 x 10^{-6} ppm/°C.

8. She hereby declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or

imprisonment, or both, under 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Tamar A. Powers

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Issued: January 9, 1996	

DECLARATION OF WILLIAM N. HOGG

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

William N. Hogg states and declares that:

1. He is a registered Patent Attorney (Reg. No. 20,156), a partner in the law firm of Calfee, Halter & Griswold LLP, Cleveland, Ohio, and an attorney of record in Application Serial No. 07/848,467 (the `467 application), filed March 9, 1992 by Ronald W. Gedney and Tamar A. Powers, (nee Tamar A. Sholtes), which application matured into the above-identified U.S. Patent (the `421 patent), assigned to IBM Corporation ("IBM").

2. He was employed by IBM from August, 1976 to July, 1987. From August of 1976 to June of 1979 he held the position of Patent Attorney at Boulder, Colorado. From June of 1979 to December of 1982 he held the position of Patent Counsel at Burlington, Vermont. From December of 1982 to July of 1987 he held the position of Intellectual Property Law Counsel at Boca Raton, Florida.

3. He has continued to provide patent services and advice to IBM from July 1987 to the present, initially as a sole practitioner, then of counsel in another law firm, and from June 1990 to present as a partner at Calfee, Halter & Griswold LLP.

4. He has worked with Ronald Gedney, one of the co-inventors of the invention disclosed and claimed in the `421 patent, on numerous patent matters. At Burlington, he was responsible for patent matters at IBM's Burlington facility, where Mr. Gedney held the position of Manager of Packaging Development, and they conferred about patent matters on a regular basis. He knows that Mr. Gedney generally understands patent practice.

5. He received an Invention Disclosure from The Endicott IP Law Department of IBM (a copy of which is enclosed, with certain dates and other non-material information redacted) for the invention disclosed and claimed in the `421 patent, with a request to prepare and file a patent application on this invention. He conferred with Mr. Gedney by telephone on several occasions during the preparation of this application. Following these conversations with Mr. Gedney, he completed and filed the `467 application on March 9, 1992 in the names of Mr. Gedney and Tamar A. Sholtes. The claims of this application were directed to packages and methods for mounting integrated circuit chips on circuit boards, with the chip being secured by solder connections to a chip carrier formed of an organic dielectric material and the chip carrier in turn being attached by solder connections to a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier. Dependent claims 6 and 12 specified that the coefficients of thermal expansion of the carrier and board should not differ by more than about 20%, and the specification stated that "in the preferred embodiment, the chip carrier and the board are both made of the above-noted glass filled epoxy FR-4 material which has a thermal coefficient of expansion of about 17-20 x 10^{-6} ppm/°C" (page 17, lines 9-13 of the `467 application; column 7, line 19 of the `421 patent). This statement was based on the first paragraph of the above identified Invention Disclosure. He believed, but did not

confirm with the inventors, that such a range of coefficients of thermal expansion would cover substantially all commercial FR-4 materials. None of the initial claims recited any specific coefficient of thermal expansion

6. He subsequently received an initial Office Action on this application (Paper No. 3, dated February 22, 1993) in which all claims were rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent 4,825,284 to Soga et al. in view of U.S. Patent 5,065,227 to Frankeny et al. The second sentence of the last paragraph on page 3 of the Office Action states: "Furthermore, the patent to Soga et al., in col. 4 lines 27 and 28 teaches that the circuit board may be made from an organic material."

7. He discussed the Office Action and references with Mrs. Powers. They noted that the statement from Soga with respect to circuit boards of organic material was an isolated statement, not supported by anything else in the patent, which discloses and claims ceramic chip carriers on ceramic circuit boards. They also noted that the materials disclosed in both Soga and Frankeny for chip carriers and circuit boards (excluding the one brief suggestion in Soga that the circuit board could be organic) had coefficients of thermal expansion significantly lower than the 17-20 x 10^{-6} ppm/°C range recited in the `467 application. He and Mrs. Powers agreed that differences between the Gedney-Sholtes invention and the disclosures of Soga and Frankeny could be emphasized by limiting the claims to a package with a chip carrier formed of an organic glass filled epoxy having a CTE of at least 17 x 10^{-6} ppm/°C, and a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier. At that time, he believed that claims reciting a coefficient of thermal expansion of at least 17 x 10^{-6} ppm/°C would cover substantially all commercial glass-filled epoxy or FR-4 circuit boards and chip carriers, and amended the claims of the `467 application accordingly.

8. The Examiner responded with a Final Office Action in which all claims remaining were rejected (page 2-32, paragraph

no. 4) under 35 U.S.C. §103 as being unpatentable over Applicant's Acknowledged Prior Art in view of US Patent 4,821,142 to Ushifusa et al. and European reference 0337686. In the paragraph running from page 3 onto page 4, beginning three lines from the bottom of page 3, the Examiner drew:

> "the applicant's attention to European ref. (0337686) where in lines 42-44 in the left column, it is stated that organic circuit boards have a coefficient of thermal expansion as large as 15 x 10^{-6} to 25 x 10^{-7} ppm/°C.[1] Furthermore in the same column in lines 31-41, gives reasons why it is desirable to use an organic material rather than ceramic material. Therefore, it is the examiner's position that the European ref. (0337686) clearly suggests using an organic material for the circuit board and that organic materials are recognized as having the claimed value of coefficient of thermal expansion." (emphasis and footnote added)

10. Applicants have never disputed that certain organic materials are recognized as having the claimed value or coefficients of thermal expansion. However, the foregoing statement glosses over the fact that the European reference, like Soga, refers to the use of an organic material for the circuit board, not for the chip carrier. This is not too surprising since the inventors listed in the Soga and Ushifusa patents and the European reference are apparently all members of a research team at Hitachi, Ltd., Tokyo. Tasao Soga is listed as an inventor in all three references and Nobuyuki Ushifusa, Hiroichi Shinohara and Satoru Ogihara are listed in two of the three.

11. None of these references, either singly or in combination, disclose or suggest that a superior package can be formed by combining an organic chip carrier with an organic circuit board having a coefficient of thermal expansion similar to the chip carrier, with encapsulated solder connections between the chip and the chip carrier, and solder connections between the chip carrier and the circuit board. This increases the difference in

[1] The figures given in lines 42-44 of the left column on page 3 of the patent are actually 150 to 250 x 10^{-7} °C, or 15 to 25 x 10^{-6} °C.

coefficients of thermal expansion between the chip and the chip carrier, which the references were trying to avoid. However, this can be dealt with by encapsulating the solder connections from the chip to the chip carrier, and the better match between the coefficients of thermal expansion of the chip carrier and circuit board yields significant advantages over prior art organic circuit board structures. As described in column 8, lines 19-45 of the `421 patent, these advantages include the ability to use larger chip carriers when desired and the ability to use smaller solder balls, based on current carrying requirements rather than on the structural strength between the chip carrier and circuit board. This in turn increases the number of I/O connections that can be made within a given area, always a matter of major importance in modern electronic packaging.

12. In response to the Final Office Action, Declarant requested reconsideration of the rejection based on Ushifusa and the European reference because the prior art does not disclose forming a chip carrier of organic glass filled material having a coefficient of thermal expansion of at least 17 x 10^{-6} ppm/°C, and joining the organic chip carrier with solder connections to an organic circuit board having a similar coefficient of thermal expansion. The limitation of a coefficient of thermal expansion of at least 17 x 10^{-6} ppm/°C was relied on because it provides a clear distinction between the ceramic chip carriers of Soga, Ushifusa and the European reference, which typically have CTE's of 6-7 x 10^{-6} ppm/°C and because he believed, based on information in the inventor's Invention Disclosure, that substantially all commercially available glass filled epoxy materials suitable for circuit boards and chip carriers had CTE's of at least 17 x 10^{-6} ppm/°C. The request for reconsideration was not successful. However, similar arguments were accepted by the Board of Appeals and US Patent 5,483,421 issued.

13. Some time after the `421 patent issued, Lawrence R. Fraley, Senior Intellectual Property Attorney, International Business Machines Corporation, Intellectual Property Law Department, requested that he review the patent and advise if it

might be possible to obtain claims which were not limited to a coefficient of thermal expansion of at least 17 x 10^{-6} ppm/°C. This was the first time that he was aware that the 17 x 10^{-6} ppm/°C limitation was thought to cover less than the inventors had the right to claim.

14. He asked James A. Rich, another patent attorney at Calfee, Halter & Griswold LLP, to review the file. He discussed the invention, the references and the prosecution with Mr. Rich, and they conferred with Mr. Gedney, who provided additional information about his knowledge, and the knowledge of others skilled in the art, with respect to coefficients of thermal expansion of materials for electronic applications. He and Mr. Rich concluded that:

A. It is apparent from the materials and information provided by Mr. Gedney, set forth in more detail in his Declaration submitted herewith, that at the time the `467 application was filed Mr. Gedney and others skilled in the electronic packaging art knew that the coefficients of thermal expansion of glass filled epoxy organic materials could be 15 x 10^{-6} ppm/°C or less. Thus, the addition of claims to materials or methods using materials with CTE's of at least 15 x 10^{-6} ppm/°C or 16 x 10^{-6} ppm/°C, and the proposed preliminary amendment adding a similar statement to the specification of this application should not be considered new matter. In re Oda, 443 F.2d 1200, 170 USPQ 268 (CCPA 1971); Ex Parte Brodbeck, 199 USPQ 230 (P.T.O.Bd. App. 1977).

B. The decision of the Board of Appeals indicates that any combination of a chip carrier and CTE having similar coefficients of thermal expansion of at least 17 x 10^{-6} ppm/°C would be patentable over the cited references. As stated in the second to fourth sentences of the paragraph running from the bottom of page 7 to the top of page 8 of the Board's Decision on Appeal:

"The examiner has provided no evidence to counter the suggestion in Ushifusa that the CTE of the chip carrier can not exceed the CTE of the chip by more

than 10 x 10^{-6} ppm/°C. , As we noted above, this limitation requires that the CTE of the chip carrier not exceed about 16 x 10^{-6} ppm/°C. Based upon the evidence before us, there is not suggestion to make the chip carrier and circuit board out of material having a CTE of at least 17 x 10^{-6} ppm/°C."

C. The Ushifusa patent indicates that the reliability of the solder joint can be maintained until the thermal expansion coefficient difference reaches 1 x 10^{-5} ppm/°C (column 5, lines 10-14). This would suggest that, with a silicon semi-conductor device having a coefficient of thermal expansion of 3.5 x 10^{-6} ppm/°C as stated in European Patent 337,686, relied upon by the Examiner, a chip carrier having a CTE of 13.5 x 10^{-6} ppm/°C will be satisfactory. However, Table 3 suggests that the deterioration begins at a lower level, i.e. before the CTE of the carrier reaches 13.2 x 10^{-6} ppm/°C. Since the statement in column 5, lines 10-15 appears to be a rounded generalization, the data in the table is more persuasive.

D. It should also be noted that table 3 does not state that the two substrates that yielded "fairly good" results had a CTE of 13.2 x 10^{-6} ppm/°C. It simply said that these substrates had CTE's between 10.7-13.2 x 10^{-6} ppm/°C. The best interpretation of Table 3 would seem to be that joint reliability with a silicon semi-conductor is likely to deteriorate with carriers having CTE's somewhere between 12-13 x 10^{-6} ppm/°C. For gallium arsenide semi-conductors, one could expect deterioration to start to occur with carriers having a CTE between about 14.5 and 15.5 x 10^{-6} ppm/°C. None of these figure are likely to encourage packaging engineers or designers to use organic materials, with their generally higher coefficients of thermal expansion, for chip carriers. Ushifusa et al. clearly do not provide any such encouragement. All of their carriers and circuit boards are ceramic. The only references to organic materials, outside of those used in the formation of the

ceramic member, is for the material between the semi-conductor and the carrier. And that material is stated to have a CTE substantially the same as the solder. European Patent 337,686 does not correct any of the deficiencies of Ushifusa et al. If anything, the European Patent does even more to discourage pursuit of applicants' claimed invention. It is true, as stated by the Examiner, that the European Patent discloses organic circuit boards. However, the semi-conductors are mounted on ceramic carriers, which are connected to the organic circuit boards by mechanical pins, mute testimony to the difficulties of connecting ceramic and organic materials with solder connections. It is difficult to see how this suggests that ceramic semi-conductors could be successfully joined to organic chip carriers with solder connections.

E. It is also not obvious from the cited references that an IC chip with fine line conductors, e.g. 0.001 inch wide and bond pads spaced close together, e.g. 0.008-0.010 inch apart, could be successfully connected to a printed circuit board having wires at least 0.005 inches wide and bond pads spaced at least 0.050 inch apart by bonding the chip to an organic chip carrier having a CTE significantly higher than the CTE of the chip, encapsulating the solder connections between the chip and carrier to absorb or reduce thermally induced stresses in these connections, and bonding the chip carrier to a circuit board made of the same organic material or another with a similar coefficient of thermal expansion. As noted above and at column 8, lines 17-45 of the `421 patent, this produces a number of very significant advantages. Neither these advantages, nor the structure and methods by which applicants produce them are disclosed or suggested by the cited references.

15. After consulting with Mr. Gedney and reviewing the materials which he provided, and reviewing the cited references, the decision of the Board of Appeals and other relevant materials with Mr. Rich, Declarant has concluded that he did not appreciate

the true nature and scope of the invention disclosed in the `467 application during its preparation or prosecution, and thus failed to prepare claims which provide the scope of protection to which applicants were entitled. He now believes that applicants were and are entitled to claim:

A. Packages and methods for mounting integrated circuit chips on a circuit board wherein the chip is bonded by solder connections to an organic chip carrier having a coefficient of thermal expansion of at least about 15 x 10^{-6} ppm/°C, with an encapsulation material encapsulating the solder connections between the chip and the carrier, with the chip carrier connected by a second set of solder connections to an organic circuit board having a coefficient of thermal expansion similar to, i.e. within 20 percent of, the coefficient of thermal expansion of the carrier.

B. Packages and methods for mounting integrated circuit chips on an organic dielectric circuit board having a coefficient of thermal expansion of at least about 15 x 10^{-6} ppm/°C, wherein the chip is bonded by solder connections to an organic chip carrier having a coefficient of thermal expansion similar to, i.e. within 20 percent of the coefficient of thermal expansion of the circuit board, with the chip carrier connected by a second set of solder connections to the organic circuit board and an encapsulation material encapsulating the solder connections between the chip and the carrier.

C. Packages and methods for mounting integrated circuit chips on a circuit board wherein the chip is bonded by solder connections to an organic chip carrier, with an encapsulation material encapsulating the solder connections between the chip and the carrier, and with the chip carrier connected by a second set of solder connections to an organic circuit board having a coefficient of thermal expansion similar to, i.e. within 20 percent of, the coefficient of thermal expansion of the carrier.

16. Paragraphs 15.A through 15.C. above summarize various aspects of the invention described in applicants' Invention Disclosure, described and claimed in the `467 application, and disclosed and claimed in the `421 patent. As stated in paragraph 6 above, the claims of the `467 application were directed to packages and methods for mounting integrated circuit chips onto circuit boards, wherein the chip is secured by solder connections to a chip carrier formed of an organic dielectric material and the chip carrier is in turn attached by solder connections to a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier. None of the references cited in the `467 application, or otherwise know to Declarant, disclose or suggest this combination. Paragraphs 15.A through 15.C outline various features that make this combination possible and enable applicants to obtain the very significant advantages provided by their invention. Since neither applicants' invention or the advantages that it provides are disclosed or suggested by the prior art the claims of the reissue application being submitted herewith, which spell out the combinations of paragraph 15.A through 15.C in greater detail, are believed to be in condition for allowance.

Respectfully submitted,

12-23-97

William N. Hogg
Reg. No. 20,156
CALFEE, HALTER & GRISWOLD LLP
800 Superior Avenue, Suite 1400
Cleveland, Ohio 44114
(216)622-8485

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Issued: January 9, 1996	

ASSOCIATE POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please recognize James A. Rich of Calfee, Halter & Griswold, Reg. No. 25,519, as associate attorney in the prosecution of the above-identified application for Letters Patent, with full power: to prosecute said application; to make alterations and amendments therein; to receive all notices, communications and said Letters Patent at the address indicated below; and to transact all business in the U.S. Patent and Trademark Office connected therewith.

Please forward all correspondence to:

James A. Rich, Esq.
Calfee, Halter & Griswold
800 Superior Avenue
1400 McDonald Investment Center
Cleveland, Ohio 44114

Please address any telephone calls to James A. Rich, Esq., at (216) 622-8636, and send any facsimile transmissions to (216) 622-8636.

Date: Jan. 07, 1998

Respectfully submitted,

By: Lawrence R. Fraley

Lawrence R. Fraley
Registration No. 26,885
IBM Corporation
Intellectual Property Law
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Endicott, NY 13760
Telephone: (607) 757-6768
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Attorney of Record

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OFFER TO SURRENDER PATENT
ASSENT OF ASSIGNEE TO SURRENDER OF PATENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

International Business Machines Corporation, owner of the entire right, title and interest in and to U.S. Patent No. 5,483,421 by virtue of an assignment from inventors Ronald W. Gedney and Tamar A. Sholtes, recorded on March 9, 1992 at Reel 6049, Frame 735, hereby assents to the surrender of said letters patent, and offers to surrender the original patent. Deferral of the surrender of the original patent until allowance of this application is respectfully requested pursuant to 37 CFR 1.178.

International Business Machines

By: Jeffrey L. Fox

Title: Manager, Information Services

Date: January 7, 1998

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CERTIFICATE UNDER 37 C.F.R. § 3.73(b)

Applicant: Gedney et al.

Application No.: USP 5,483,421 Filed: Issued January 9, 1996

For: IC CHIP ATTACHMENT

International Business Machines Corporation, a corporation of New York,

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel 6049, Frame 735, or for which a copy thereof is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application identified above, to the current assignee as shown below:

1. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date : January 7, 1998

Name : Jeffrey L. Forman

Title : Manager, Information Services

Signature: Jeffrey L. Forman